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(54) SOLID-STATE IMAGE PICKUP DEVICE

(57)Abstract:

PROBLEM TO BE SOLVED: To solve a problem of a conventional solid-state image pickup device, whose pixel is configured with one photodiode, 4 transistors(TRs) and one capacitor, that cannot have utilized only either of a field shutter function and a kTC (k is Boltzman's constant, T is absolute temperature and C is a capacitance) noise cancel function.

SOLUTION: After resetting a capacitor Ce by a TR M1, a charge transfer TR M5 is conductive to transfer charges obtained by photoelectric conversion at a photo diode PD to the capacitor Ce, where the charges are stored. Then each TR M5 is turned off simultaneously for all the pixels and Trs M1, M3 of pixels on the same row are conductive, to provide a prescribed level to a CDS(correlation dual sampling) circuit 5. Succeedingly, a TR M6 is conductive and the TR M3 is turned on to output a signal corresponding to the charges, by a field shutter function stored in the capacitor Ce to

the CDS circuit 5. Thus, the CDS circuit transfer can cancel kTC noise.

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2.**** shows the word which can not be translated.

3.In the drawings, any words are not translated.

CLAIMS

[Claim(s)]

[Claim 1] A photodiode and the transducer from which said photodiode changes into potential change the charge obtained by carrying out photo electric conversion, A pixel equipped with the transistor for reset for resetting said transducer and an output means to output the potential of said transducer to the exterior Or two or more arrays are carried out at the shape of single dimension Rhine, and two in the condition of only background noise that the signal level and signal level from said pixel have not ridden are sampled. the shape of a 2-dimensional matrix -- In the solid state camera equipped with the noise canceller which removes a noise by taking the difference The capacitor for accumulating a charge between said photodiodes and said transducers into said pixel temporarily is formed. Between said capacitors and said photodiodes, the 1st transistor for a charge transfer Between said capacitors and said transducers, the 2nd transistor for a charge transfer is prepared, respectively. After outputting

the potential of only the background noise on which a signal has not ridden with said output means and saving after reset of said transducer with said transistor for reset at said noise canceller, Carry out photo electric conversion with said photodiode, and the charge which transmitted to said capacitor and was accumulated in it is transmitted to all pixel coincidence through said 2nd transistor for a charge transfer to said transducer through said 1st transistor for a charge transfer. The new potential produced in this transducer as a result is outputted to said noise canceller with said output means. The solid state camera characterized by taking difference with the potential of only said background noise beforehand saved in this noise canceller, and having the control means which takes out the difference as a true signal.

[Claim 2] A photodiode and the transducer from which said photodiode changes into potential change the charge obtained by carrying out photo electric conversion, A pixel equipped with the transistor for reset for resetting said transducer and an output means to output the potential of said transducer to the exterior Or two or more arrays are carried out at the shape of single dimension Rhine, and two in the condition of only background noise that the signal level and signal level from said pixel have not ridden are sampled. the shape of a

2-dimensional matrix -- In the solid state camera equipped with the noise canceller which removes a noise by taking the difference The 1st transistor for a charge transfer connected to said photodiode into said pixel, It is approached and prepared between the 2nd transistor for a charge transfer connected to said transducer, and said 1st and 2nd transistors for a charge transfer. The MOS gate which accumulates the charge from said photodiode is prepared directly under it. After resetting said transducer with said transistor for reset After outputting the potential of only the background noise on which a signal has not ridden with said output means and saving at said noise canceller, Carry out photo electric conversion with said photodiode, and the charge which transmitted directly under said MOS gate and was accumulated in all pixel coincidence through said 1st transistor for a charge transfer is transmitted to said transducer through said 2nd transistor for a charge transfer. The new potential produced in this transducer as a result is outputted to said noise canceller with said output means. The solid state camera characterized by taking difference with the potential of only said background noise beforehand saved in this noise canceller, and having the control means which takes out the difference as a true signal.

[Claim 3] The solid state camera according to claim 1 or 2 characterized by connecting the 2nd transistor for reset which is switched to the node of said photodiode and said 1st transistor for a charge transfer to the timing of arbitration, and resets said photodiode at the time of ON. [Claim 4] A photodiode and the 1st transistor for reset connected to said photodiode, The transducer from which said photodiode changes into potential change the charge obtained by carrying out photo electric conversion, The 2nd transistor for reset for resetting said transducer, Or two or more arrays are carried out at the shape of single dimension Rhine. a pixel equipped with an output means to output the potential of said transducer to the exterior -- the shape of a 2-dimensional matrix -- Two in the condition of only background noise that the signal level and signal level from said pixel have not ridden are sampled. The 1st transistor for a charge transfer which is the solid state camera equipped with the noise canceller which removes a noise by taking the difference, and was connected to said photodiode and the 1st transistor for reset into said pixel, It is approached and prepared between the 2nd transistor for a charge transfer connected to said transducer, and said 1st and 2nd transistors for a charge transfer. The MOS gate which accumulates the charge from said photodiode is prepared directly under it. After

resetting said photodiode with said 1st transistor for reset Said 1st transistor for a charge transfer is set to ON in the condition of impressing the 1st electrical potential difference for making said 1st transistor for reset off, and setting the potential [directly under] of said MOS gate as the middle level at the time of max and min to said MOS gate. Since the charge by which photo electric conversion was carried out is transmitted and stored up directly under said MOS gate with the 1st shutter time amount and said photodiode, said 1st transistor for a charge transfer is made off. After resetting said photodiode with said 1st transistor for reset again Said 1st transistor for a charge transfer is set to ON in the condition of impressing the 2nd electrical potential difference for making said 1st transistor for reset off, and setting the potential [directly under] of said MOS gate as larger level than said 1st electrical potential difference to said MOS gate. The solid state camera characterized by having the control means which makes off said 1st transistor for a charge transfer since the charge by which photo electric conversion was carried out is transmitted and stored up directly under said MOS gate with the 2nd shutter time amount shorter than said 1st shutter time amount and said photodiode.

DETAILED DESCRIPTION

[Detailed Description of the Invention]

[0001]

[Field of the Invention] This invention relates to the CMOS image sensors which started the solid state camera, especially had the store-and-forward section in

the pixel.

[0002]

[Description of the Prior Art] It roughly divides into the conventional solid state camera, and there are two, a CCD method and a CMOS sensor method, in it. The difference among both is in the place referred to as how to tell the information on the charge of the photodiode instead of the photodiode which changes light into a charge out of each photo detector.

[0003] A CCD method transmits directly the charge generated in the photodiode to the exterior by the charge coupled device (CCD:charge coupled device). On the other hand, a CMOS sensor method is outputted to the component exterior through the amplifier in which the information on the potential by the charge generated in the photodiode was prepared corresponding to each photodiode. Since the pixel structure of this CMOS sensor method can be created in the almost same process as the usual CMOS-LSI process, Rhine for CMOS-LSI can be used for it as it is, and it has the merit that an area sensor and other CMOS circuits can be intermingled.

[0004] On the other hand, there is a trouble that a fixed pattern noise is loud compared with a CCD method in a CMOS sensor method. The fixed pattern

noise mainly originates in the variation in the threshold electrical potential difference of the transistor for amplifier.

[0005] Drawing 7 shows the block diagram of an example of the conventional solid state camera. The most general CMOS image sensors are shown, a pixel 211 - 233 grades are arranged in the shape of a 2-dimensional matrix, and this conventional solid state camera is the perpendicular shift register 1 among these pixels 211-233. Actuation of two or more (arranged horizontally) pixels of each line is controlled for every line (it usually goes to a lower line from the upper line). The signal from each pixels 211-233 It is inputted into a load and a noise canceller 3, and after noise cancellation actuation is carried out, a transistor T1 - T3 turn on one by one with the level shift register 4, and the signal of each train is outputted as an image pick-up signal. Usually, as for processing, processing progresses to a left train from a right train. In addition, a row and column can also be arranged conversely. Moreover, it is also possible to arrange a pixel the shape not of a 2-dimensional matrix but in the shape of [of one train] single dimension Rhine.

[0006] The noise canceller called a CDS circuit with a pixel is attached to this conventional solid state camera, i.e., the conventional CMOS image sensors.

There is this in order to remove background noise (mainly variation of the threshold electrical potential difference of the transistor for amplifier of a pixel) when the signal is not contained from the output signal of a pixel.

[0007] Drawing 8 shows the representative circuit schematic of an example for 1 pixel of the conventional solid state camera called CMOS image sensors. The same sign is given to the same component as drawing 7 among this drawing. One pixel 2a consists of the transistor M1 for reset by which the source was connected to the N type layer of one photodiode PD and photodiode PD, a transistor M2 for magnification by which the gate was connected to the N type layer of Photodiode PD, and a transistor M3 for a transfer in drawing 8 . Transistors M1, M2, and M3 are MOS mold field-effect transistors (FET), and are usually FET of an n channel.

[0008] The source of a transistor M2 is connected to the double correlation sampling (CDS) circuit 5 and the load 6 through the transistor M3 with a switch function, and a transistor M3 operates as a source follower circuit. The CDS circuit 5 consists of two capacitors C1 and C2 and two switches S1 and S2. The non-grounded side terminal of a capacitor C1 is connected to the source of a transistor M3 through a switch S1 and a capacitor C2 at a serial. Switch S1

side-edge child C2a of a capacitor C2 is connected to reference voltage Vref through a switch S2, and switch S1 side-edge child C1b of a capacitor C1 is connected to the signal output line through the switch S3. [0009] The CDS circuit 5 and a load 6 are the circuitry parts for pixel 1 train the load of drawing 7 , and among noise cancellers 3. The CDS circuit 5 samples two in the condition of only background noise that the signal level and signal level from a pixel have not ridden, and carries out the role of the noise canceller which removes a noise by taking the difference. Moreover, a current regulator circuit is usually used for a load 6.

[0010] Next, actuation of equipment is explained conventionally [this]. Now, pixel 2a in drawing 8 presupposes that it is the pixel of a train with the line of somewhere middle which are not the top line and the lowest line. First, ON and a transistor M3 are made off and a transistor M1 makes a reset condition the terminal T1 by the side of the N type layer of Photodiode PD. Potential of the terminal T1 at this time is made into a reset electrical potential difference (Vdd-Vthrst). Here, Vdd is supply voltage and Vthrst is the threshold electrical potential difference of a transistor M1. In the state of this reset, since the transistor M3 is off, there is no output from this pixel 2a in a train signal line.

[0011] Next, incidence of the light from a photographic subject is carried out to Photodiode PD, and photo electric conversion is made to perform, where a transistor M1 is made off. Thereby, the charge according to the amount of incident light is accumulated in Photodiode PD. The capacity Cpxl in a terminal T1 serves as the capacity Cpd of Photodiode PD, and gate capacitance Camp of a transistor M2 from the diffusion capacitance Crst of a transistor M1, and the stray capacity Cf of wiring. If the amount Q of net charge occurs in Photodiode PD, potential change of only **V=Q/Cpxl will occur in this terminal T1. On the other hand, the CDS circuit 5 is processing the output signal of the pixel of other lines in the meantime.

[0012] Processing of the output signal of the pixel (not shown) of the continued line of pixel 2a which the CDS circuit 5 is observing is ended, and if a processing result is outputted through the switch S3 closed with the level shift register 4, the CDS circuit 5 will start processing of pixel 2a currently observed. The CDS circuit 5 performs its reset action first.

[0013] That is, switches S1 and S2 are closed and terminal C2a and potential of terminal C1b are made into the reference potential Vref. If a high-level electrical potential difference is impressed to the gate of a transistor M3 in this condition

and M3 is turned ON, the potential (Vdd-Vthrst+**V) of the terminal T1 of Photodiode PD will be amplified with a transistor M2, and the potential which lets the drain of a transistor M3 and the source pass further (Vdd-Vthrst-Vthamp+**V) will be outputted to a train signal line (that is, terminal C2b). Thereby, the potential difference of (Vdd-Vthrst-Vthamp+**V-Vref) is built over a capacitor C2. Here, Vthamp is the threshold electrical potential difference of a transistor M2.

[0014] Then, a switch S2 is opened, a reset electrical potential difference is impressed to the gate of a transistor M1, and M1 is set to ON. Then, since the potential of the terminal T1 of Photodiode PD serves as (Vdd-Vthrst), the potential of terminal C2b serves as (Vdd-Vthrst-Vthamp). It means that, as for terminal C2b, potential had changed by this only in (Vdd-Vthrst-Vthamp)-(Vdd-Vthrst-Vthamp+**V) =-** V. This is equal to a part for the electrical-potential-difference change by the side of the terminal T1 of Photodiode PD. Therefore, only the amount of [by the photo electric conversion of Photodiode PD] electrical-potential-difference change is able to take out purely by a series of above-mentioned actuation.

[0015] Consequently, as for the potential of terminal C2a (= terminal C1b), only

the proportionality component to which capacitors C1 and C2 were connected with the serial by electrical-potential-difference change part **V changes. It is got blocked. Vref- {**V-C1/(C1+C2)} (1)

It becomes. Then, a switch S1 is opened and it supposes that it is off, and a processing result is held to a capacitor C1, and it stands by to it. Then, a transistor M3 becomes off and that of the output from pixel 2a is lost. Then, the processing result of (1) type which the switch S3 was closed to a certain timing, and was held with the level shift register 4 of drawing 7 at the capacitor C1 is outputted as a pixel signal. Then, a switch S3 opens, it is supposed that it is off, and it returns to the first reset condition. The actuation same also about each pixel as the above is performed. [0016] However, in the CMOS image sensors of drawing 8 , a shutter function poses a problem. That is, in CCD, since carriers are moved from a photodiode to a transfer field all at once at a certain moment, the image information obtained from CCD has synchronia in all the pixels in 1 screen, and CCD essentially has a shutter function.

[0017] On the other hand, since the CMOS image sensors of drawing 8 are read in order for every line, the image created using this information shows the time amount which is different for every line. Therefore, it will become the bent image

if a still picture is taken out. The shutter of such image shifted in time is called rolling shutter in many cases.

[0018] The shutter which makes the still picture to which it was equal in time on the other hand is called field shutter in many cases. One method of giving a field shutter function with the conventional CMOS image sensors of the configuration of drawing 8 only with the function of a rolling shutter is preparing a mechanical shutter. That is, a mechanical shutter is prepared in addition to a component, and only a certain specific time amount should open a shutter. However, by this approach, cost becomes high and photography of an animation is difficult.

[0019] In order to carry out with a field shutter function, it is indispensable to have the switch which takes out a certain instantaneous image information to coincidence by all pixels, and the are recording section which stores it temporarily. Then, a transistor M4 and capacity Ce are usually applied to a picture element part like drawing 9 , and it realizes. The same sign is given to the same component as drawing 8 among this drawing, and the explanation is omitted. In drawing 9 , an end is connected to a terminal T1 with MOS transistor M4 by which a drain and the source were further connected to pixel 2a of drawing 8 between the N type layer of Photodiode PD, and the terminal T1, and

pixel 2b has the description in the point of having added further the capacitor Ce for adjustment by which the other end was grounded. A transistor M4 takes charge of a shutter function, and Capacitor Ce takes charge of an are recording function. In addition, the gate capacitance of a transistor M2 etc. may be enough as Capacitor Ce, and it does not need to form especially the capacitor Ce in that case. The actuation at the time of making it such a configuration is shown below.

[0020] Pixel 2b presupposes that it is the pixel of a train with the line of somewhere middle which are not the top line of a picture element part, and the lowest line. In explaining the cycle of actuation of a pixel, it carries out [that the output of the now last information just finished and]. In this condition, transistors M1, M3, and M4 are off. The potential of the terminal T1 at this time is (Vdd-Vthrst). Here, Vdd is supply voltage and Vthrst is the threshold electrical potential difference of a transistor M1. Since the terminal T1 was not connected anywhere but has floated electrically at this time, it is still reset potential. Moreover, since the transistor M3 is off, there is no output from pixel 2b in a train signal line. Photo electric conversion is performed in the photodiode PD which the transistor M4 has also become off on the other hand, therefore is electrically separated from the terminal T1. Performing photo electric conversion in this way,

it is waiting for pixel 2b until the information on the pixel of all the lines below itself is read. [0021] In this way, if the signal of all pixels is read and predetermined time amount passes after photo-electric-conversion initiation, the transistors M4 of all pixels turn on all at once. Then, the charge accumulated in the N type layer side of Photodiode PD is transmitted to a terminal T1 by all pixels at coincidence. Consequently, the charge of Photodiode PD is lost and PD is reset. After a transfer is completed, a transistor M4 becomes off and Photodiode PD starts photo electric conversion again.

[0022] The capacity Cpxl of a terminal T1 consists of Capacitor Ce, gate capacitance Camp of a transistor M2, and the diffusion capacitance Crst of a transistor M1 and the stray capacity Cf of wiring. Therefore, if the transmitted amount of net charge sets to Q, potential change of only **V=Q/Cpxl will take place to a terminal T1. In addition, since the carrier transmitted is an electron, Charge Q is a negative value, therefore **V is also a negative value. Since the potential of a terminal T1 was (Vdd-Vthrst) before the charge transfer, after a charge transfer is set to (Vdd-Vthrst+**V).

[0023] After a transfer of a charge is completed by all pixels, the CDS circuit 5 performs signal processing for every line. While processing other lines, pixel 2b

currently observed stands by holding to the capacitor Ce by which the charge was connected to the terminal T1. And the CDS circuit 5 starts processing of pixel 2b currently observed. First, its reset action is performed. That is, as mentioned above, switches S1 and S2 are closed and potential of terminal C2a and terminal C1b is made into the reference potential Vref. At this time, a switch S3 is opened and is off. If a high-level electrical potential difference is impressed to the gate of a transistor M3 in this condition and M3 is turned ON, the potential of (Vdd-Vthrst-Vthamp+**V) will be outputted to a train signal line (that is, terminal C2b). Thereby, the potential difference of (Vdd-Vthrst-Vthamp+**V-Vref) is built over a capacitor C2.

[0024] Then, if a switch S2 is opened and it turns OFF, since it is not anywhere connected with terminal C2a (= terminal C1b), will be floated electrically. Here, a transistor M1 is once turned ON, it turns OFF after predetermined time, and a terminal T1 is reset. Then, since the potential of a terminal T1 serves as (Vdd-Vthrst), the potential of terminal C2b serves as (Vdd-Vthrst-Vthamp). Therefore, it means that, as for the potential of terminal C2b, only (Vdd-Vthrst-Vthamp)-(Vdd-Vthrst-Vthamp+**V) =-** V had changed. This is a component proportional to the amount Q of charges generated in Photodiode

PD. Therefore, only the amount of [by the photo electric conversion of Photodiode PD] signal is able to take out purely by a series of above-mentioned actuation.

[0025] Consequently, as for the potential of terminal C2a (= terminal C1b), only the proportionality component to which capacitors C1 and C2 were connected with the serial by change part-**V changes. That is, only the same value as the aforementioned (1) formula changes. Then, a switch S1 is opened and it supposes that it is off, and a processing result is held to a capacitor C1, and it stands by to it. Then, a transistor M3 becomes off and that of the output from pixel 2b is lost. Then, the processing result of (1) type which the switch S3 was closed to a certain timing, and was held with the level shift register 4 of drawing 7 at the capacitor C1 is outputted as a pixel signal. Then, a switch S3 opens, it is supposed that it is off, and it returns to the first condition. In this way, 1 cycle of a series of processings is completed, and the same actuation as the following is repeated. [0026]

[Problem(s) to be Solved by the Invention] However, there is a serious trouble in the CMOS image sensors with a field shutter function which are the conventional solid state cameras shown in above-mentioned drawing 9 . That is, with the

conventional equipment of drawing 9 , after transmitting the charge of Photodiode PD to the terminal T1 reset beforehand, generating potential with it and outputting it out of a pixel, it is reset again and made into the level of the criteria for cancellation. That is, the reset action of different timing is used in the time of outputting a signal, and the time of outputting the background. Thus, when the electrical potential difference by the reset action of another timing is compared, there is a problem that a kTC noise is not removed.

[0027] This kTC noise is a noise resulting from an electronic thermal motion. For example, making potential of a certain capacity C into a certain potential V is giving the electron of Charge q to the capacity C only several predeterminedn piece (or it removing) like drawing 10 . Several of the n can be expressed like a degree type.

[0028]

n=V/(C-q) (2)

If switch S4 is opened as concrete actuation after it closes a bond and switch S4 through Resistance R and switch S4 to the power source of an electrical potential difference V and sufficiently long time amount passes capacity C as shown in drawing 10 , an above-mentioned number of electrons are stored in

capacity C, and both ends have an electrical potential difference V.

[0029] However, since the electron is carrying out thermal motion at random in fact, while having closed switch S4, the number of the electron number in capacity C of electronic increases more than n at a certain time, and variation is in **** that it is smaller than n when another, in time. For this reason, when switch S4 is opened and it turns OFF, or there will be few electron numbers which remained in capacity C then than n. [chance] This variation serves as a noise called a kTC noise, and appears. kTC -- k: -- the thing of a Boltzmann's constant, T:absolute temperature, and C:capacity -- it is -- the noise level Vi -- rms -- Vi=root (kT/C) (3)

It is expressed. (3) As shown in a formula, it is the description to depend for this noise level Vi only on temperature and capacity.

[0030] Therefore, in the terminal T1 of the CMOS image sensors of drawing 9 , if the thing of the timing of two different reset is compared, noise level Vi1 and Vi2 different, respectively can remain, and cannot cancel. When there is no correlation in such noise level Vi1 and Vi2 and it compares the thing which is not such correlated, a kTC noise is doubled root2, and it is Vi'=root (2 kT/C). (4)

It becomes.

[0031] As shown in the above-mentioned (3) types and (4) types, a kTC noise becomes so large that capacity is small. For this reason, with the configuration of drawing 8 and drawing 9 , if the pixel is made detailed, it will become impossible to take large Cpxl gradually, and a kTC noise will become large.

[0032] Here, a kTC noise is estimated quantitatively. For example, suppose that the capacity Cpxl of a terminal T1 was set to 8fF(s). The numeric value of these 8fF(s) is a numeric value which wore a touch of reality, when pixel size becomes below 5-micrometer opening. At this time, kTC noise part Vi' is set to about 1mV at the room temperature of T= 300 degrees K. If a noise considers [the maximum amplitude of a signal] only as a kTC noise by 2V, the S/N ratio of the above-mentioned CMOS image sensors with a field shutter function will be set to 46dB. Since it is said that the S/N ratio of a CCD method is 60dB or more, it is only a kTC noise and it turns out that the engine performance is considerably inferior as compared with a CCD method.

[0033] In the CMOS image-sensors configuration of the easiest structure of aforementioned drawing 8 , since the capacity Cpd of Photodiode PD is quite large in the capacity of a terminal T1, a problem is smaller than the case of the configuration of drawing 9 . However, it is impossible to remove a kTC noise with

the configuration of drawing 8 .

[0034] Since there are more transistors than the configuration of drawing 8 when it is made detailed, it becomes impossible on the other hand, to cleave a big capacity gradually for a terminal T1 in the conventional CMOS image sensors of the configuration of drawing 9 . Therefore, the configuration of drawing 9 of the need of controlling a kTC noise is higher. With the configuration of this drawing 9 , if not a field shutter but rolling shutter actuation is performed, a kTC noise is removable.

[0035] Rolling shutter actuation is performed as follows with the configuration of drawing 9 . First, transistors M4 and M3 presuppose that it is off. At this time, there is no output from this pixel 2b in train signal-line C2b. At this time, incidence of the light is carried out to the photodiode PD of pixel 2b, photo electric conversion is performed, and a charge is accumulated in Photodiode PD. Moreover, the CDS circuit 5 is processing the signal of the component of other lines.

[0036] Next, processing of the line currently observed starts. A transistor M1 turns on and a terminal T1 is reset by (Vdd-Vthrst). Then, a transistor M1 is turned off. Then, a transistor M3 is set to ON. At this time, a transistor M4 is still

off. Thereby, a signal (Vdd-Vthrst-Vthamp) when a terminal T1 is reset is outputted to a train signal line. In the CDS circuit 5, switches S1 and S2 are closed, and the potential difference of (Vdd-Vthrst-Vthamp-Vref) is saved to a capacitor C2.

[0037] Next, a switch S2 is opened and suppose that it is off. Then, a transistor M4 is set to ON. Thereby, the charge of Photodiode PD flows into a terminal T1 through the drain of a transistor M4, and the source. The capacity Cpxl of a terminal T1 serves as Capacitor Ce and gate capacitance Camp of a transistor M2 from the diffusion capacitance Crst of a transistor M1, and the stray capacity Cf of wiring. If the amount of net charge of Photodiode PD is set to Q, potential change of only **V=Q/Cpxl will occur in this terminal T1. The potential of this terminal T1 is amplified with a transistor M2, lets the transistor M3 which is ON pass, and is outputted to a train signal line as (Vdd-Vthrst-Vthamp+**V).

[0038] Thereby, since change of the potential of terminal C2b is set to (Vdd-Vthrst-Vthamp+**V)-(Vdd-Vthrst-Vthamp)=+**V, potential Vref+ {**V-C1/(C1+C2)} proportional to it appears in terminal C1b. This potential is outputted to the level shift register 4. Then, a transistor M3 is made off and it considers as the first reset condition.

[0039] If it does in this way, since reset will be performed only once but background noise will be removed from a signal in the same reset action, a kTC noise can also be removed. Since there is such a property, a configuration like drawing 9 is used in little rolling shutter actuation of a noise rather than for field shutter actuation in many cases.

[0040] Thus, since the are recording function part and the charge electrical-potential-difference conversion function part had been independent the photoelectrical load conversion function part of Photodiode PD, and temporarily [charge], respectively with neither of the conventional solid state cameras, drawing 8 nor drawing 9 , In the solid state camera of the pixel configuration which consists of one photodiode PD like drawing 8 , and three transistors M1-M3 The three above-mentioned function parts are united, and while there are the features of being constitutionally very simple, a field shutter function and a kTC noise cancellation function cannot be realized as the result, but there is a problem that the high-definition still picture to which it was equal in time cannot be obtained. [0041] Moreover, in the solid state camera of the pixel configuration which serves as one photodiode PD and four transistors M1-M4 which were shown in drawing 9 from one capacitor Ce, while the still picture to which it was

equal in time with a field shutter function can be obtained, there is a problem that only one of a field shutter function and the kTC noise cancellation functions can be used.

[0042] This invention was made in view of the above point, and aims at offering the solid state camera which can realize a field shutter function and a kTC noise cancellation function to coincidence.

[0043] Moreover, other purposes of this invention are to make area of a photodiode small and offer the solid state camera of a configuration advantageous to detailed-izing.

[0044]

[Means for Solving the Problem] The transducer which changes into potential change the charge obtained by a photodiode and a photodiode carrying out photo electric conversion in order that this invention may attain the above-mentioned purpose, A pixel equipped with the transistor for reset for resetting a transducer and an output means to output the potential of a transducer to the exterior Or two or more arrays are carried out at the shape of single dimension Rhine, and two in the condition of only background noise that the signal level and signal level from a pixel have not ridden are sampled. the

shape of a 2-dimensional matrix -- In the solid state camera equipped with the noise canceller which removes a noise by taking the difference The capacitor for accumulating a charge between a photodiode and a transducer into a pixel temporarily is formed. Between a capacitor and a photodiode, the 1st transistor for a charge transfer Between a capacitor and a transducer, the 2nd transistor for a charge transfer is prepared, respectively. After outputting the potential of only the background noise on which a signal has not ridden with an output means and saving after reset of a transducer with the transistor for reset at a noise canceller, Carry out photo electric conversion with a photodiode, and the charge which transmitted to the capacitor and was accumulated in it is transmitted to all pixel coincidence through the 2nd transistor for a charge transfer to a transducer through the 1st transistor for a charge transfer. Difference with the potential of only the background noise which outputted the new potential produced in the transducer as a result to the noise canceller with the output means, and saved it beforehand in the noise canceller is taken, and it considers as the configuration which has the control means which takes out the difference as a true signal.

[0045] After accumulating in a capacitor the charge obtained by carrying out

photo electric conversion to coincidence with the photodiode of all pixels in this invention, After making the potential of only the background noise on which it faces outputting to the exterior through an output means, the transistor for reset and an output means are operated, and a signal has not ridden send out and save to a noise canceller By outputting the signal corresponding to the charge accumulated in the capacitor to a noise canceller through an output means from a transducer, only the signal component proportional to the charge produced by the photo electric conversion of a photodiode in the noise canceller can be taken out.

[0046] In order to attain the above-mentioned purpose, moreover, this invention The 1st transistor for a charge transfer connected to the photodiode into the pixel, It is approached and prepared between the 2nd transistor for a charge transfer connected to the transducer, and the 1st and 2nd transistors for a charge transfer. The MOS gate which accumulates the charge from a photodiode is prepared directly under it. After outputting the potential of only the background noise on which a signal has not ridden after resetting a transducer with the transistor for reset with an output means and saving at a noise canceller, Carry out photo electric conversion with a photodiode, and the charge which

transmitted directly under the MOS gate and was accumulated in all pixel coincidence through the 1st transistor for a charge transfer is transmitted to a transducer through the 2nd transistor for a charge transfer. Difference with the potential of only the background noise which outputted the new potential produced in the transducer as a result to the noise canceller with the output means, and saved it beforehand in the noise canceller is taken, and it considers as the configuration which has the control means which takes out the difference as a true signal.

[0047] After accumulating the charge obtained by carrying out photo electric conversion to coincidence with the photodiode of all pixels in this invention directly under the MOS gate, After outputting the potential of only the background noise on which it faces outputting to the exterior through an output means, the transistor for reset and an output means are operated, and a signal has not ridden with an output means and making it save at a noise canceller By outputting the signal corresponding to the charge accumulated directly under the MOS gate to a noise canceller through an output means from a transducer, only the signal component proportional to the charge produced by the photo electric conversion of a photodiode in the noise canceller can be taken out.

[0048] Here, it is switched to the node of a photodiode and the 1st transistor for a charge transfer to the timing of arbitration, and reset of a photodiode can be performed to the timing of arbitration by connecting the 2nd transistor for reset which resets a photodiode at the time of ON.

[0049] In order to attain the above-mentioned purpose, moreover, this invention A photodiode and the 1st transistor for reset connected to the photodiode, The transducer from which a photodiode changes into potential change the charge obtained by carrying out photo electric conversion, A pixel equipped with the 2nd transistor for reset for resetting a transducer and an output means to output the potential of a transducer to the exterior Or two or more arrays are carried out at the shape of single dimension Rhine, and two in the condition of only background noise that the signal level and signal level from a pixel have not ridden are sampled. the shape of a 2-dimensional matrix -- The 1st transistor for a charge transfer which is the solid state camera equipped with the noise canceller which removes a noise by taking the difference, and was connected to a photodiode and the 1st transistor for reset into the pixel, The 2nd transistor for a charge transfer by which the end was connected to the output means, and the 2nd transistor for reset connected to the 2nd transistor for a charge transfer and

output means, respectively, It is approached and prepared between the 1st and 2nd transistors for a charge transfer, and the MOS gate which accumulates the charge from a photodiode directly under it is established in each of each pixel. After resetting a photodiode with the 1st transistor for reset The 1st transistor for a charge transfer is set to ON in the condition of impressing the 1st electrical potential difference for making the 1st transistor for reset off, and setting the potential [directly under] of the MOS gate as the middle level at the time of max and min to the MOS gate. The 1st shutter time amount, Since the charge by which photo electric conversion was carried out is transmitted and stored up directly under the MOS gate with a photodiode, the 1st transistor for a charge transfer is made off. After resetting a photodiode with the 1st transistor for reset again The 1st transistor for a charge transfer is set to ON in the condition of impressing the 2nd electrical potential difference for making the 1st transistor for reset off, and setting the potential [directly under] of the MOS gate as larger level than the 1st electrical potential difference to the MOS gate. Since the charge by which photo electric conversion was carried out is transmitted and stored up directly under the MOS gate with the 2nd shutter time amount shorter than the 1st shutter time amount and a photodiode, it considers as the

configuration which has the control means which makes the 1st transistor for a charge transfer off. [0050] In this invention, the charge which carried out photo electric conversion to the charge which carried out photo electric conversion with the photodiode by the 1st shutter time amount of the longer one with the photodiode by the 2nd shutter time amount of the shorter one can be added directly under the MOS gate.

[0051]

[Embodiment of the Invention] Next, the gestalt of operation of this invention is explained with a drawing. Drawing 1 shows the representative circuit schematic of the 1-pixel circuit of the gestalt of operation of the 1st of the solid state camera which becomes this invention. The same sign is given to the same component as drawing 8 and drawing 9 among this drawing. With the gestalt of the 1st operation shown in drawing 1 , compared with pixel 2b of drawing 9 , an MOS mold field-effect transistor (FET) and one capacitor are added, respectively, and pixel 2c is made one photodiode, five transistors, and 2 capacitor configurations. Namely, as for pixel 2c, the N type layer side of Photodiode PD is connected to the source of the transistor M1 for reset, and the gate of a transistor M2 in the node (terminal) T1 through the drain of a transistor M5, the source, the drain of a

transistor M6, and the source, respectively. [0052] Moreover, the common node of transistors M5 and M6 is grounded through Capacitor Cex. Furthermore, the terminal T1 is grounded through Capacitor Ce. Furthermore, the source of a transistor M2 is connected to the CDS circuit 5 and the load 6 through the drain of the transistor M3 for an output, and the source, respectively. In addition, Capacitor Cex consists of N-diffusion layers made for example, on p substrate front face. Moreover, especially when the sum total of gate capacitance Camp of a transistor M2, the diffusion capacitance Crst of a transistor M1, and the stray capacity Cf of wiring is enough as the capacity Cpxl of a terminal T1, it is not necessary to form Capacitor Ce. The capacity Cpxl of a terminal T1 constitutes the transducer which transforms into an electrical potential difference the charge mentioned above with Capacitor Ce.

[0053] Next, actuation of the gestalt of this operation is explained. Here, pixel 2c presupposes that it is the pixel of a train with the line of somewhere middle which are not the top line of a picture element part, and the lowest line. Moreover, switching control of each transistors M1, M3, M5, and M6 is performed based on the signal from the control circuit which is not illustrated. [0054] It begins from the place said [that the output of the last signal of this pixel 2c has just finished as a

starting point of operating cycle explanation, and]. In this condition, transistors M1 and M6 are off, and a terminal T1 is in the condition of having floated electrically. In the last cycle, Photodiode PD carried out photo electric conversion to the terminal T1, and the charge transmitted through transistors M5 and M6 remains in it as it is. The transistor M3 has also become off and there is no output from this pixel 2c to a train signal line.

[0055] On the other hand, the transistor M5 has also become off, and Photodiode PD performs photo electric conversion in the condition of having dissociated from others electrically, and is accumulating the charge. Moreover, the charge which suited Capacitor Cex is transmitted to the terminal T1 through the transistor M6, and is in the condition that there is no charge in Capacitor Cex.

[0056] It is waiting for pixel 2c to end the processing whose CDS circuit 5 is the pixel of other lines in such the condition. After signal read-out from all pixels is completed, transistors M5 turn on all at once by all pixels including pixel 2c. Then, the charge Q accumulated in Photodiode PD is transmitted to each capacitor Cex through each transistor M5 at coincidence by all pixels. Consequently, the charge of Photodiode PD is lost and is reset. After charge transfer termination, it is supposed that a transistor M5 is off, again, photo

electric conversion of the photodiode PD is carried out, and it starts are recording of a charge.

[0057] Then, pixel 2c stands by, while the CDS circuit 5 is carrying out processing which is the pixel of other lines. If processing of pixel 2c currently observed starts, pixel 2c will perform the reset action of a terminal T1. That is, the high-level signal from the control circuit which is not illustrated is impressed to the gate electrode of a transistor M1, and turns ON M1. At this time, transistors M3 and M6 are still off. Consequently, the potential of a terminal T1 serves as (Vdd-Vthrst). Here, Vdd is supply voltage and Vthrst is the threshold electrical potential difference of a transistor M1.

[0058] Then, the signal to the gate electrode of a transistor M1 serves as a low level, and M1 is made off. Thereby, return and a reset action complete a terminal T1 in the condition of having floated electrically. Since kTC noise component Vktc rides on a terminal T1 at this time, the potential of a terminal T1 serves as (Vdd-Vthrst+Vktc). Although Vktc was not specified during explanation of the conventional technique, it decides to be shown in order to show clearly that it is removable with the gestalt of this operation. [0059] On the other hand, the preparations for carrying out signal processing of pixel 2c also in the CDS circuit

5 are made. That is, switches S1 and S2 are closed and terminal C2a and C1b are made into a reference potential Vref. Since M3 is set to ON by impressing a high-level signal from the control circuit which is not illustrated to the gate electrode of a transistor M3 in this condition, the potential of (Vdd-Vthrst+Vktc-Vthamp) is outputted to a multiple-message-transmission number output line, i.e., terminal C2b. Here, Vthamp is the threshold electrical potential difference of the transistor M2 for magnification. Consequently, the potential difference of (Vdd-Vthrst+Vktc-Vthamp-Vref) is built over a capacitor C2.

[0060] Next, the CDS circuit 5 opens a switch S2, presupposes that it is off, and changes terminal C2a (= terminal C1b) into the condition of having floated. Here, it is set to ON by impressing a signal with a transistor M6 high-level from the control circuit which is not illustrated to the gate electrode. Then, the charge Q currently held at Capacitor Cex is transmitted to a terminal T1 through a transistor M6. The transistor M6 after the completion of a charge transfer is made off. Consequently, a charge is lost to Capacitor Cex and it will be in the condition of having been reset.

[0061] On the other hand, the potential change by Charge Q arises for a terminal

T1. Although the capacity Cpxl of a terminal T1 consists of the capacity of Capacitor Ce, gate capacitance Camp of a transistor M2, and the diffusion capacitance Crst of a transistor M1 and the stray capacity Cf of wiring, when Charge Q enters here, potential change of **V=Q/Cpxl occurs. Therefore, the potential of a terminal T1 is set to (Vdd-Vthrst+Vktc+**V).

[0062] If potential change takes place to a terminal T1, it will be amplified by the source follower circuit with a transistor M2, and will be told through the transistor M3 which is in an ON state further at a multiple-message-transmission number output line, i.e., terminal C2b. Thereby, the potential of terminal C2b is set to (Vdd-Vthrst+Vktc-Vthamp+**V). That is, potential change produced in terminal C2b is (Vdd-Vthrst+Vktc-Vthamp+**V)-(Vdd-Vthrst+Vktc-Vthamp)=**V, is influenced only of the component by the amount Q of charges by the photo electric conversion of Photodiode PD, and does not have the effect of a kTC noise.

[0063] According to potential change of this terminal C2b, potential change of proportionality part Vref+ {**V-C1/(C1+C2)} to which capacitors C1 and C2 were connected with the serial produces terminal C2a (= terminal C1b) which floated electrically and which is a condition. Then, a switch S1 is opened, it supposes

that it is off, and the processing result which is the above-mentioned potential change is held to a capacitor C1. And it is supposed that a transistor M3 is off and the output from pixel 2c is lost. Then, a switch S3 is set to ON with the level shift register which is not illustrated, and the processing result of pixel 2c currently held at the capacitor C1 is outputted as a pixel signal through a switch S3. Then, a switch S3 is opened again, it is supposed that it is off, and one cycle in this pixel 2c is completed. As for after, the same thing is again repeated from the beginning. [0064] In addition, explanation of actuation of the gestalt of the above-mentioned operation is an example, and is not limited to this. For example, what is necessary is to perform reset with the transistor M1 of a terminal T1 by the above-mentioned explanation, just before outputting the reset potential of a terminal T1, but just to perform it once to [somewhere in] the next signal output actuation, after it is not limited to this and the last signal output finishes. For example, immediately after the last signal output finishes, a transistor M1 is turned ON, and it may be made to perform the reset action of a terminal T1 first of all.

[0065] Moreover, although reset of Capacitor Cex is performed by transmitting the stored charge of Cex completely by the above-mentioned explanation, it

cannot transmit, if there is too much stored charge, and the phenomenon in which a charge remains in Cex may arise, and it may serve as an after-image. For this reason, before turning on a transistor M5 and transmitting a charge to Capacitor Cex from Photodiode PD, transistors M1 and M6 are turned on once, and it may be made to perform actuation which resets Capacitor Cex compulsorily.

[0066] thus, the background noise out of the signal [according to the gestalt of this operation] according to a charge transfer of Photodiode PD in the CDS circuit 5 -- it is (Vdd-Vthrst-Vthamp+Vktc) -- it is removed, and since electrical-potential-difference change part **V proportional to the amount Q of net charge produced by the photo electric conversion of Photodiode PD can take out to multiple-message-transmission number output line C2b purely, the cancellation function of a kTC noise is realizable.

[0067] Moreover, it is also possible only for predetermined time amount to hold a charge to Capacitor Cex. Furthermore, with the gestalt of this operation, since the charge obtained by carrying out photo electric conversion of the light which carried out incidence at coincidence to the photodiode of all the pixels containing Photodiode PD is transformed into an electrical potential difference and he is

trying to output it, a field shutter function can be realized and the still picture in the same time of day can be obtained. As mentioned above, a high-definition still picture can be picturized compared with the former. [0068] By the way, although the area of a pixel is restricted, when the number of transistors is increased rapidly, according to it, the area of a photodiode will decrease to it. Then, the amount Q of charges generated with a photodiode will decrease, and the sensibility to brightness will become low as image sensors. However, with the configuration of the gestalt of this operation, the fall of the area of the above-mentioned photodiode does not become disadvantageous, but works advantageously rather.

[0069] That is, with the gestalt of this operation, since it can be expressed with **V=Q/Cpxl, change **V of the potential of a terminal T1 can make a charge transfer factor high, if Cpxl is made small. Therefore, sensibility will become fixed if only the rate to which the area of a photodiode became small makes Cpxl small. Furthermore, the more it makes capacity Cpxl small, since sensibility becomes high, the more it becomes advantageous.

[0070] On the other hand, since a kTC noise will become large with the conventional configuration shown in drawing 8 or drawing 9 if capacity Cpxl is

made small as shown in (3) types and (4) types, in the former, Cpxl cannot be made small. However, if it is made the configuration of the gestalt of this operation, since removal of field shutter actuation and a kTC noise will be attained at coincidence, Cpxl can be made small and area of a photodiode can also be made small. Therefore, it is a configuration advantageous to detailed-izing.

[0071] Next, the gestalt of operation of the 2nd of this invention is explained. The description of this invention is in the configuration which makes the photodiode which performs photo electric conversion, the site which holds temporarily the carrier which the photodiode generated, and the site which transforms the charge of a carrier into an electrical potential difference become independent, respectively. Here, not a capacitor but an option is possible for the configuration of the site which holds a carrier temporarily. Then, the gestalt of this 2nd operation holds a carrier by the MOS gate.

[0072] Drawing 2 shows the representative circuit schematic for 1 pixel of the gestalt of operation of the 2nd of the solid state camera which becomes this invention. The same sign is given to the same component as drawing 1 among this drawing. With the gestalt of this 2nd operation, instead of the capacitor Cex

of drawing 1 , as shown in drawing 2 , the gate Mccd of MOS is approached and arranged to transistors M5 and M6, and the description is in the point using 2d of pixels of the structure where a charge can be held under the MOS gate Mccd. The potential at this time and the situation of migration of a charge are shown in drawing 3 . In addition, like drawing 1 , since Ce is the addition capacity for adjustment, omitting is a function. [0073] Next, actuation of the gestalt of this operation is explained with drawing 2 and drawing 3 . In addition, 2d of pixels presupposes that it is the pixel of a train with the line of somewhere middle which are not the top line of a solid state camera, and the lowest line. It begins from the place said [that the output of the last signal of 2d of this pixel has just finished as a starting point of operating cycle explanation, and]. [0074] In this condition, transistors M1 and M6 are off, and a terminal T1 is in the condition of having floated electrically. In the last cycle, Photodiode PD carried out photo electric conversion to the terminal T1, and a transistor M5, Mccd, and the charge transmitted through M6 remain in it as it is. The transistor M3 has also become off and there is no output from 2d of this pixel to a train signal line. On the other hand, the transistor M5 also serves as OFF, and Photodiode PD performs photo electric conversion like drawing 3 (A) in the condition of having dissociated from

others electrically, and is accumulating the charge like drawing 3 (B). Moreover, Mccd has also become off, and it is in the condition that a charge is not stored and it is in a condition without a charge. [0075] It is waiting for 2d of pixels to end the processing whose CDS circuit 5 is the pixel of other lines in such the condition. If signal read-out from all pixels is completed and predetermined time amount passes since photo-electric-conversion initiation, a transistor M5 and the MOS gates Mccd turn on all at once by all pixels including 2d of pixels like drawing 3 (C). Then, the charge Q accumulated in Photodiode PD is transmitted in the direction [directly under] of each MOS gate Mccd through each transistor M5 at coincidence by all pixels. Consequently, the charge of Photodiode PD is lost and is reset.

[0076] As shown in drawing 3 (D) after charge transfer termination, a transistor M5 is set to OFF and all charges are transmitted directly under the MOS gate Mccd. Again, photo electric conversion of the photodiode PD is carried out, and it starts are recording of a charge. On the other hand, Mccd has become with ON and continues holding a charge under the gate. 2d of pixels is in such a condition, and while the CDS circuit 5 is processing the pixel of other lines, they continue standing by.

[0077] Then, if processing of 2d of pixels currently observed starts, 2d of pixels will perform the reset action of a terminal T1. That is, the high-level signal from the control circuit which is not illustrated is impressed to the gate electrode of a transistor M1, and turns ON M1. At this time, transistors M3 and M6 are still off. Consequently, the potential of a terminal T1 serves as (Vdd-Vthrst). Here, Vdd is supply voltage and Vthrst is the threshold electrical potential difference of a transistor M1.

[0078] Then, the signal to the gate electrode of a transistor M1 serves as a low level, and M1 is made off. Thereby, return and a reset action complete a terminal T1 in the condition of having floated electrically. Since kTC noise component Vktc rides on a terminal T1 at this time, the potential of a terminal T1 serves as (Vdd-Vthrst+Vktc).

[0079] On the other hand, the preparations for carrying out signal processing of 2d of pixels also in the CDS circuit 5 are made. That is, switches S1 and S2 are closed and terminal C2a and C1b are made into a reference potential Vref. Since M3 is set to ON by impressing a high-level signal from the control circuit which is not illustrated to the gate electrode of a transistor M3 in this condition, the potential of (Vdd-Vthrst+Vktc-Vthamp) is outputted to a

multiple-message-transmission number output line, i.e., terminal C2b. Here, Vthamp is the threshold electrical potential difference of the transistor M2 for magnification. Consequently, the potential difference of (Vdd-Vthrst+Vktc-Vthamp-Vref) is built over a capacitor C2.

[0080] Next, the CDS circuit 5 opens a switch S2, presupposes that it is off, and changes terminal C2a (= terminal C1b) into the condition of having floated. Here, by impressing a signal with a transistor M6 high-level from the control circuit which is not illustrated to the gate electrode, as shown in drawing 3 (E), M6 is set to ON. On the other hand, if the signal of a low level is impressed to the MOS gate Mccd, the charge Q which was directly under Mccd will be transmitted to a terminal T1 through a transistor M6. As the transistor M6 after the completion of a charge transfer is set to OFF and shown in drawing 3 (F), all charges are transmitted to a terminal T1.

[0081] Consequently, the potential change by Charge Q arises for a terminal T1. Although the capacity Cpxl of a terminal T1 consists of the capacity of Capacitor Ce, gate capacitance Camp of a transistor M2, and the diffusion capacitance Crst of a transistor M1 and the stray capacity Cf of wiring, when Charge Q enters here, potential change of **V=Q/Cpxl occurs. Therefore, the potential of a

terminal T1 is set to (Vdd-Vthrst+Vktc+**V).

[0082] If potential change takes place to a terminal T1, it will be amplified by the source follower circuit with a transistor M2, and will be told through the transistor M3 which is in an ON state further at a multiple-message-transmission number output line, i.e., terminal C2b. Thereby, the potential of terminal C2b is set to (Vdd-Vthrst+Vktc-Vthamp+**V). That is, potential change produced in terminal C2b is (Vdd-Vthrst+Vktc-Vthamp+**V)-(Vdd-Vthrst+Vktc-Vthamp)=**V, is influenced only of the component by the amount Q of charges by the photo electric conversion of Photodiode PD, and does not have the effect of a kTC noise.

[0083] According to potential change of this terminal C2b, potential change of proportionality part Vref+ {**V-C1/(C1+C2)} to which capacitors C1 and C2 were connected with the serial produces terminal C2a (= terminal C1b) which floated electrically and which is a condition. Then, a switch S1 is opened, it supposes that it is off, and the processing result which is the above-mentioned potential change is held to a capacitor C1. And it is supposed that a transistor M3 is off and the output from pixel 2c is lost. [0084] Then, a switch S3 is set to ON with the level shift register which is not illustrated, and the processing result of 2d of

pixels currently held at the capacitor C1 is outputted as a pixel signal through a switch S3. Then, a switch S3 is opened again, it is supposed that it is off, and one cycle in 2d of this pixel is completed. As for after, the same thing is again repeated from the beginning. [0085] In addition, explanation of actuation of the gestalt of the above-mentioned operation is an example, and is not limited to this. For example, what is necessary is to perform reset with the transistor M1 of a terminal T1 by the above-mentioned explanation, just before outputting the reset potential of a terminal T1, but just to perform it once to [somewhere in] the next signal output actuation, after it is not limited to this and the last signal output finishes. [0086] Since the signal and background noise which are deducted and carried out by the above actuation are taken with the reset potential performed to the same timing, a kTC noise is canceled. Moreover, since the charge all pixel same time of day carried out [the charge] photo electric conversion is outputted from a level shift register one by one, a field shutter function is realized. [0087] Next, the gestalt of operation of the 3rd of this invention and the gestalt of the 4th operation are explained. The representative circuit schematic of 1 pixel of the gestalt of operation of the 3rd of the solid state camera with which drawing 4 becomes this invention, and drawing 5 show the representative circuit schematic

of 1 pixel of the gestalt of operation of the 4th of the solid state camera which becomes this invention. The same sign is given to the same component as drawing 1 and drawing 2 among both drawings, and the explanation is omitted.

[0088] Reset of Photodiode PD was performed with the gestalt of the old 1st and the 2nd operation by the action of transmitting a carrier (charge). However, by this approach, reset of Photodiode PD will become the exposure time which is 1 time and was always fixed to the 1 field. Since shutter speed cannot be freed now, it is convenient if the transistor for photodiode reset which became independent to Photodiode PD is attached.

[0089] Then, in the gestalt of operation of the 3rd of this invention shown in drawing 4 , the transistor M7 for photodiode reset is formed in the pixel of the gestalt of the 1st operation, and the transistor M7 for photodiode reset is formed in the pixel of the gestalt of the 2nd operation with the gestalt of operation of the 4th of this invention shown in drawing 5 . That is, in drawing 4 and drawing 5 , the N type layer of Photodiode PD is connected to supply voltage Vdd through the source of the MOS mold field-effect transistor M7, and a drain. [0090] Thereby, in drawing 4 and drawing 5 , if a high-level reset signal is impressed to the gate of a transistor M7, a transistor M7 is turned on, and through the drain of

a transistor M7, and the source, supply voltage Vdd will be impressed to the N type layer of Photodiode PD, and will reset this. That is, even if the carrier of Photodiode PD does not finish being transmitted, Photodiode PD is resettable to the timing of arbitration by turning on a transistor M7 to the timing of arbitration. Therefore, with the gestalt of the 3rd and the 4th operation, shutter time amount can be set up freely. [0091] Moreover, with the gestalt of operation of the 4th of drawing 5 , since a part for a carrier attaching part is constituted from the CCD type MOS gate Mccd, the potential of the part in which the carrier directly under the MOS gate Mccd is held with the potential of the MOS gate Mccd can be moved freely. Thereby, an advantageous mode of operation can be set up.

[0092] Next, other modes of operation of the gestalt of operation of the 4th of this invention are explained. As an approach of opening a dynamic range, the method of adding the short thing of shutter time amount and a long thing is learned from before. The long things of shutter time amount are for example, 10msec(s), and short things are for example, 0.5msec(s).

[0093] A bright place will become ********, although a dark place is well reflected as everyone knows when shutter time amount is long. On the other hand, when shutter time amount is short, a dark place will become ******** although

projection of a bright place becomes good. Therefore, if both information is added, a dark place and a bright place can be copied together.

[0094] Hereafter, actuation in other modes of the gestalt this 4th operation is concretely explained based on the configuration shown in drawing 6 (A). The same sign is given to the same component as drawing 5 among this drawing (A). In addition, illustration of transistors M7, M1-M3 is omitted. First, after resetting Photodiode PD, photo electric conversion between the time amount Tl with longer shutter time amount is performed. Then, the 1st potential from which the potential of the channel of the MOS gate Mccd becomes abbreviation half [of the potential when applying the potential of Vdd to the gate electrode of Mccd] is applied to the gate electrode of Mccd.

[0095] If a transistor M5 is turned on in this condition, as shown in drawing 6 (B), a carrier (charge) will be transmitted to the bottom of the MOS gate Mccd through a transistor M5. Then, a transistor M5 is made off. Thereby, as shown in drawing 6 (B), the potential of the potential of a transistor M5 becomes high, and a charge is held directly under the MOS gate Mccd. [0096] Next, after resetting Photodiode PD again, only Ts with short shutter time amount performs photo electric conversion. As a black dot shows to drawing 6 (C) typically, a charge is

accumulated in Photodiode PD by this photo electric conversion. Then, the 2nd larger potential, for example, Vdd, than the 1st potential is impressed to the gate electrode of the MOS gate Mccd. Thereby, the potential of the potential directly under Mccd becomes still deeper than the last condition. [0097] When a transistor M5 is set to ON, as it is shown in drawing 6 (D) in this condition, the charge accumulated in Photodiode PD at the MOS gate Mccd flows through a transistor M5, and the charge of this shutter time amount Ts is added to the charge at the time of the last shutter time amount Tl directly under Mccd. Thus, if the made charge is outputted to Tl, the signal with which the dynamic range spread can be outputted.

[0098] In addition, by old explanation, it is NMOS. It will be PMOS, if N type and P type are replaced and the direction of an electrical potential difference is made reverse, although FET is used. Of course, effectiveness with the same said of FET is acquired.

[0099]

[Effect of the Invention] As explained above, after accumulating the charge obtained by carrying out photo electric conversion to coincidence with the photodiode of all pixels in the charge storage sections, such as a capacitor and

the MOS gate, according to this invention, After facing outputting to the exterior through an output means, operating the transistor for reset, and an output means and sending out predetermined potential to a noise canceller By outputting the signal corresponding to the charge accumulated in the charge storage section to a noise canceller through an output means Since only the signal component proportional to the charge produced by the photo electric conversion of a photodiode in the noise canceller was taken out, Field shutter actuation by all pixel coincidence photo electric conversion and removal (kTC noise rejection) of the background noise in a noise canceller can be performed to coincidence, and, thereby, a high-definition still picture can be picturized.

[0100] Moreover, since the charge which carried out photo electric conversion to the charge which carried out photo electric conversion with the photodiode by the 1st shutter time amount of the longer one with the photodiode by the 2nd shutter time amount of the shorter one was added directly under the MOS gate according to this invention, the signal with which the dynamic range spread can be outputted.

[0101] Furthermore, since according to this invention the electrical potential difference in inverse proportion to the capacity in the common connection

terminal of the transistor for reset, the 2nd transistor for a charge transfer, and an output means constitutes so that it may be generated for this common connection terminal and the above-mentioned capacity can make area of a photodiode small corresponding to making it small, it can consider as a configuration advantageous to detailed-izing.

DESCRIPTION OF DRAWINGS

[Brief Description of the Drawings]

[Drawing 1] It is the representative circuit schematic for 1 pixel of the gestalt of operation of the 1st of this invention.

[Drawing 2] It is the representative circuit schematic for 1 pixel of the gestalt of operation of the 2nd of this invention.

[Drawing 3] It is drawing showing the potential of the important section of drawing 2 , and the situation of migration of a charge.

[Drawing 4] It is the representative circuit schematic of 1 pixel of the gestalt of operation of the 3rd of this invention.

[Drawing 5] It is the representative circuit schematic of 1 pixel of the gestalt of operation of the 4th of this invention.

[Drawing 6] It is drawing explaining actuation in other modes of the gestalt operation of the 4th of this invention.

[Drawing 7] It is the block diagram of an example of the whole solid state camera.

[Drawing 8] It is the representative circuit schematic for 1 pixel of an example of the conventional solid state camera.

[Drawing 9] It is the representative circuit schematic for 1 pixel of other examples of the conventional solid state camera.

[Drawing 10] It is drawing showing making potential of a certain capacity C into a certain potential V.

[Description of Notations]

1 Perpendicular Shift Register

2c, 2d The 1st, pixel of the gestalt of the 2nd operation

3 Load and Noise Canceller

4 Level Shift Register

5 CDS Circuit

6 Load

PD Photodiode

M1 Field-effect transistor for reset

M2 Field-effect transistor for magnification (output means)

M3 Field-effect transistor for an output (output means)

M5, M6 Transistor for a charge transfer (the 1st, 2nd transistor for a charge transfer)

M7 Field-effect transistor for photodiode reset

Mccd MOS gate

Cex Capacitor for charge storages

Ce Capacitor for capacity adjustment of a transducer

S1, S2, S3 Switch

T1 Terminal